CLAIMS

What is claimed is:

1. A method for forming an offset spacer adjacent a CMOS gate structure comprising the steps of:

providing a substrate comprising a gate structure;

forming at least one oxide layer overlying the substrate;

forming at least one nitride layer overlying the at least one oxide layer;

etching the at least one nitride layer in a first dry etching process to expose a first portion of the at least one oxide layer;

carrying out a wet etching process to remove the first portion of the at least one oxide layer; and,

etching the at least one nitride layer in a second dry etching process to remove the at least one nitride layer leaving a second portion of the at least one oxide layer to form an oxide offset spacer along sidewalls of the gate structure.

2. The method of claim 1, wherein at least the second dry etching process comprises an etching chemistry having a fluorine to carbon ratio of about 3 or less.

3. The method of claim 1, wherein the first and second dry etching processes comprise an etching chemistry having a fluorine to carbon ratio of about 3 or less.

4. The method of claim 1, wherein at least the second dry etching process comprises CF_4 and fluorohydrocarbon plasma source gases.

5. The method of claim 1, wherein at least the second dry etching process comprises CF_4 and CH_2F_2 plasma source gases.

6. The method of claim 1, wherein at least the second dry etching process comprises CF_4, CH_2F_2, and O_2 plasma source gases.

7. The method of claim 1, wherein at least the second dry etching process comprises CF_4, fluorohydrocarbon, and O_2 plasma source gases with an additional plasma source gas selected from the group consisting of argon, helium, and nitrogen.

8. The method of claim 1, wherein at least the second dry etching process comprises a downstream plasma etching process.

9. The method of claim 1, wherein the at least one nitride layer is selected from the group consisting of silicon nitride and silicon oxynitride.

10. The method of claim 1, wherein the step of wet etching comprises an HF containing wet etching solution.

11. The method of claim 1, wherein at least the second dry etching process is carried with a nitride to oxide selectivity of greater than about 130.

12. The method of claim 1, wherein the width of the oxide offset spacer is formed at a width of less than about 150 Angstroms.

13. A method for forming an oxide offset spacer along a CMOS gate structure sidewall comprising the steps of:

providing a silicon substrate comprising a polysilicon gate structure;

forming a silicon oxide layer overlying the substrate;

forming a silicon nitride layer overlying the silicon oxide layer;

etching the silicon nitride layer in a first dry etching process comprising fluorohydrocarbons to expose a first portion of the silicon oxide layer;

carrying out a wet etching process to remove the first portion of the silicon oxide layer; and,

etching the silicon nitride layer in a second dry etching process comprising fluorohydrocarbons having a silicon nitride to silicon oxide etch selectivity of greater than about 130 to remove the silicon nitride layer leaving a second portion of the silicon oxide layer to form a silicon oxide offset spacer.

14. The method of claim 13, wherein the second dry etching process comprises an etching chemistry having a fluorine to carbon ratio of about 3 or less.

15. The method of claim 13, wherein the second dry etching process comprises CF_4 and CH_2F_2 plasma source gases.

16. The method of claim 13, wherein the second dry etching process comprises CF_4, CH_2F_2, and O_2 plasma source gases.

17. The method of claim 13, wherein the second dry etching process comprises CF_4, fluorohydrocarbon, and O_2 plasma source gases with an additional plasma source gas selected from the group consisting of argon, helium, nitrogen, and mixtures thereof.

18. The method of claim 13, wherein the second dry etching process comprises a downstream plasma etching process.

19. The method of claim 13, wherein the step of wet etching comprises an HF containing wet etching solution.

20. The method of claim 13, wherein the second dry etching process is carried with a silicon nitride to silicon oxide etch selectivity of greater than about 150.

21. The method of claim 13, wherein the silicon oxide offset spacer is formed at a width of less than about 150 Angstroms.

22. A semiconductor device, comprising:

a substrate;

a gate structure formed overlying the substrate;

an offset spacer formed along the sidewall of the gate structure; and

wherein the width of the offset spacer is less than 1bout 150 angstroms.

23. The semiconductor device of claim 22, wherein the offset spacer comprises at least one oxide layer.

24. The semiconductor device of claim 22, wherein the gate structure is a polysilicon gate structure.